Method for fabricating nanometer gate in semiconductor device using thermally reflowed resist technology

Background
Field of the invention

The invention relates to a method for fabricating nanometer gate semiconductor device using thermally reflowed photoresist technology and, more specifically, to a method for fabricating nanometer gate semiconductor device using combination of an electron beam photolithography and a thermally reflowed photoresist technology.

Related arts of the invention

Conventionally, in order to promote the performance of the high frequency semiconductor device, such as higher cut-off frequency and maximum resonance frequency, except to develop the structure of the element with a high mobility, the shrinkage of the gate width is also another approach to achieve, where the nanometer photolithography is a critical technique to manufacture such a nanometer gate semiconductor device.

In the literature of IEEE Electron Device Lett. 22(2001) 367, entitled "Ultra-Short 25-nm-Gate Lattice-Matched InAlAs/InGaAs HEMTs within the Range of 400Ghz Cut-off Frequency", proposed by Yoshimi Yamashita, Akira Endoh, Keisuke Shinohara, Masataka Hikashiwaki, Kohki Hikosaka and Takashi Mimura, described that the high performance devices that operate in the millimeter-wave (30 to 300GHz) and sub-millimeter-wave (300GHz to 3THz) frequency ranges will be major elements of the future communication system. InP-based InAlAs/InGaAs high electron mobility transistors (HEMTs) are the most promising candidates, since this material system provides high electron mobilities, high saturation velocities, and high sheet electron densities. In both field-effect transistors (FETs) and HEMTs high-speed characteristics can essentially be obtained by reducing the gate length.

However, as described on above, due to the short gate width, it is not easy to attach the gate on the surface of the substrate which may cause the problem of gate loose. Consequently, how to fixedly attach the gate on the substrate

becomes another subject for the research. Furthermore, the influence of the shape of gate in DC and high frequency features of the device is also worthy of study. However, these two subjects are not falled in the scope of the invention.

Therefore, it is necessary to develop a method for fabricating a sub-micron, i.e. nanometer gate, capable of using a simplified heating process for fabrication of a nanometer gate having line width smaller than 0.1 micrometer (order of nanometers) without any expensive apparatus (e.g. the yellow light photolithography apparatus) and high technical level of manufacturing process, which makes it possible to achieve a fine line width and simplify the manufacturing process, so as to reduce the cost and improve the yield effectively.

Summary of the invention

In view of the above described conventional problems, the object of the invention is to provide a method for fabricating nanometer gate semiconductor device using thermally reflowed photoresist technology, capable of using a simplified heating process for fabrication of a nanometer gate having line width smaller than 0.1 micrometer without any expensive apparatus and high technical level of manufacturing process, which makes it possible to achieve a fine line width and simplify the manufacturing process, so as to reduce the cost and improve the yield effectively.

To achieve the above object, according to one aspect of the invention, a method for fabricating nanometer gate semiconductor device using thermally reflowed photoresist technology is provided, comprising the steps of :

(i) spin-coating two layers of photoresists on a substrate in order, where a bottom layer of photoresist, one of the two layers of photoresists, is a polymeric photoresist which has a lower sensitivity and a higher resolution with respect to an electron beam, and a top layer of photoresist, one of the two layers of photoresists, is another polymeric photoresist which has a higher sensitivity and a lower resolution with respect to the electron beam;

(ii) heating the two layers of photoresists for curing these layers by way of using a hotplate;

(iii) using photolithography with a high accelerating voltage in an electron beam direct writing manner to expose a pattern on the two layers of photoresists for forming a gate;

(iv) using a developer and an etchant for developing and etching in order

to form a recess on the gate;

(v) plating a metallic layer on the recess of the gate by way of using an electron gun evaporation technique; and

(vi) removing the photoresists to obtain the gate,

characterized in that after the etching of the recess of the gate, the photoresists are reflowed by using a hot plate heating manner within a predetermined period of time and temperature, such that the recess of the gate is formed with a nanometer-sized width.

Further, according to the above aspect of the invention, the bottom layer of photoresist is a PMMA (polymethyl methacrylate) photoresist or a LOR (lift-off) photoresist.

Further, according to the above aspect of the invention, the top layer of photoresist is a P(MMA-MAA) (poly(methacrylate-methyl acrylic acid)) photoresist or a PMGI (polymethylglutarimide) photoresist.

Further, according to the above aspect of the invention, the metallic layer is a Ti/Pt/Au Schottky metallic layer.

Further, according to the above aspect of the invention, the predetermined period of time and temperature for the reflow of said photoresists are about 75 seconds and about 125 ^{0}C, respectively, and the heating manner employs a bottom heating manner.

Further, according to the above aspect of the invention, the heating temperatures for the bottom and top layers of said photoresists are about 250 ^{0}C and 180 ^{0}C, respectively, and the heating time of each layer is about 3 minutes.

Further, according to the above aspect of the invention, the step of removing the photoresists employs acetone to remove said photoresists.

Further, according to the above aspect of the invention, the recess of the gate is T-shaped.

Further, according to the above aspect of the invention, the substrate is a GaAs substrate.

Further, according to the above aspect of the invention, the developer is a

MIBK : IPA = 1 : 3 high resolution developer.

Further, according to the above aspect of the invention, the photoresists are at least two layers of multi-layered photoresists structure containing PMMA, LOR, PMGI, and P(MMA-MAA).

Brief description of the drawing

The invention will present in detail the following description of the preferred embodiments with reference to the following drawings, in that the same reference number represents the identical element, wherein

Fig. 1(a) to 1(d) are schematic views, showing manufacturing process steps according to an embodiment of the invention;

Fig. 2 is a flow chart, illustrating the method according to the embodiment of the invention;

Fig. 3 is a cross section view, showing an electron micrograph of the photoresist before performing the thermal reflow, according to the embodiment of the invention;

Fig. 4 is a cross section view, showing an electron micrograph of the photoresist after performing the thermal reflow, according to the embodiment of the invention;

Fig. 5 a cross section view, showing an electron micrograph of the finished nanometer gate according to the embodiment of the method of the invention ; and

Fig. 6 is a graph, showing the relationship of the thermal reflow time and temperature versus the critical dimension of the gate according to the embodiment of the method of the invention.

Description of the preferred embodiments

Hereinafter, the invention will now be described more fully with reference to the accompanying drawings, in which preferred embodiments of the invention are shown and the same reference numeral indicates the identical element. However, the person who is skillful in the art should appreciate that

these embodiments are just illustrative of the invention and should not be construed as being limited to the embodiments set forth herein. Note that the modifications and variations can be made without departing from the spirit and scope of the invention.

Referring to Fig. 1(a) to 1(d), show manufacturing process steps of a structural embodiment according to the method for fabricating a nanometer gate of the invention, and referring to FIG. 2, shows a flow chart of the embodiment according to the method of the invention. Firstly,
in step S1 of Fig. 2, a substrate 1, such as GaAs is prepared. However, the present invention is not confined in a kind of the substrate, for example these substrates typically used in the fabrication of semiconductor devices can be implemented in accordance with the invention. In steps S2 and S3, two layers of photoresist structures are spin-coated on the GaAs substrate in order by using a spin-coating machine, and baked. Among others, a bottom layer of photoresist, one of the two layers of photoresists, is a polymeric photoresist such as PMMA, which has a lower sensitivity and a higher resolution with respect to an electron beam, and a top layer of photoresist, one of the two layers of photoresists, is another polymeric photoresist such as P(MMA-MAA), which has a higher sensitivity and a lower resolution with respect to the electron beam. In order to obtain an optimal resolution for the photoresist, these two layers of the photoresists are heated by a hot plate, respectively, such that these two layers of the photoresists are cured. The heating temperatures of which are about 250 ^{0}C and 180 ^{0}C, respectively, and the heating time of each layer is around 3 minutes, as shown in Fig. 1(a). However, the present invention is not confined in a kind of the photoresist, for example a PMGI (polymethylglutarimide) photoresist and a LOR (lift-off) photoresist can replace the P(MMA-MAA) (poly(methacrylate-methyl acrylic acid)) photoresist and PMMA (polymethyl methacrylate) photoresist, respectively.

Next, in step S4, an electron beam photolithography with 40,000 volts accelerating voltage is used in a directly writing manner to expose a photoresist structure of a gate having a T-shaped pattern. Then, in step S5,
using a high resolution developer (MIBK : IPA = 1 : 3) to develop and etch a T-shaped recess, as the structure shown in Fig. 1(b), where the T-shaped gate structure is employed in order to allow the lower end of the linewidth to be smaller and the upper end of the gate contact much larger.

Then, in step S6, the photoresists are reflowed by using a hot plate through

an appropriate period of heating time and temperature to form a desired nanometer gate width. Preferably, the heating time and temperatures for the reflow are about 75 seconds and 125 ^{0}C, respectively. However, the present invention is not limited to these conditions and not specified in using the hot plate, either. Instead of the hot plate, the oven can also be used for the reflow of the photoresists, as shown in Fig. 1(c).

Finally, in step S7, a metal layer, such as Ti/Pt/Au Schottky metallic layer, is evaporated by the electron gun evaporation system or deposited on the recess of the gate; and in step S8, excess of the photoresists and metal are removed by performing a lift-off process using acetone so as to obtain a nanometer width of the gate, as shown in Fig. 1(d).

As described on above, using a combination of the electron beam photolithography and the thermally reflowed photoresist technique, it is capable of utilizing a simplified heating process (for example, the hot plate or oven heating manner) to fabricate a nanometer gate having line width smaller than 0.1 micrometer without any expensive apparatus and high technical level of manufacturing process, which makes it possible to achieve a fine line width and simplify the manufacturing process, so as to reduce the cost and improve the yield effectively. Also, it allows the semiconductor device to obtain a higher cut-off frequency and a larger oscillating frequency.

The Fig. 3 to 5 are examples of implementations in accordance with the aspect of the present invention, performed by the inventor. Among others,
Fig. 3 is a cross section view, showing an electron micrograph of the photoresist before performing the thermal reflow, according to the embodiment of the method of the invention, where the width of the recess of the gate is about 163.1 nanometers, as indicated by *X; Fig. 4 is a cross section view, showing an electron micrograph of the photoresist after performing the thermal reflow, according to the embodiment of the invention, where the width of the recess of the gate is about 30.59 nanometers; Fig. 5 is a cross section view, showing an electron micrograph of the finished nanometer gate according to the embodiment of the method of the invention, where the line width of gate matel is about 50.0 nanometers.

Fig. 6 is a graph, showing the relationship of the thermal reflow time and temperature versus the critical dimension of the gate according to the embodiment of the method of the invention. The heating time and temperature of the hot plate can be well-controlled, such that the nanometer width of the

recess of the gate can be obtained through the thermal reflow of the photoresists in order to fit with the further process.

Having described the preferred embodiments of the invention on above, however, they are not intended to be the limit of the invention. It should be noted that modifications and variations of the invention can be made by a person who is skillful in the art in light of the above teachings. It is therefore to be understood that various changes, equivalents and modifications may be made in the particular examples of the invention without departing from the scope and the spirit of the invention as outlined by the appended claims.

List of the reference numerals

1	GaAs substrate
2'	bottom layer of photoresist
3	top layer of photoresist
4	recess
5	gate mate